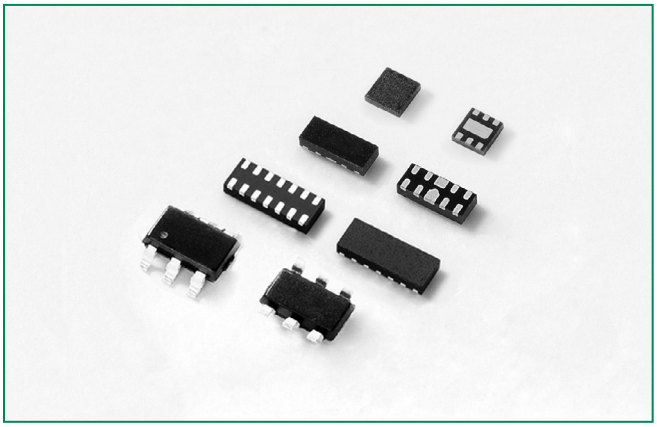
Littelfuse
Expertise Applied | Answers Delivered

TVS Diode Arrays (SPA® Diodes)

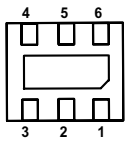
Low Capacitance ESD Protection - SP3012 Series

SP3012 Series 0.5pF Diode Array for USB3.0

AUTOMOTIVE GRADE | RoHS | Pb GREEN

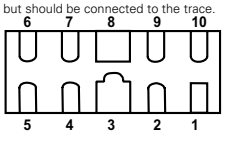


Pinout

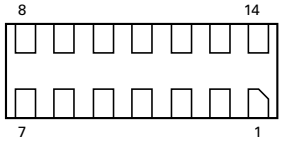


SP3012-03UTG

*Pins 6, 7, 9, 10 are not internally connected but should be connected to the trace.

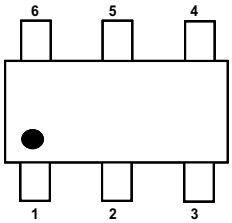


SP3012-04UTG (AEC-Q101 Qualified)



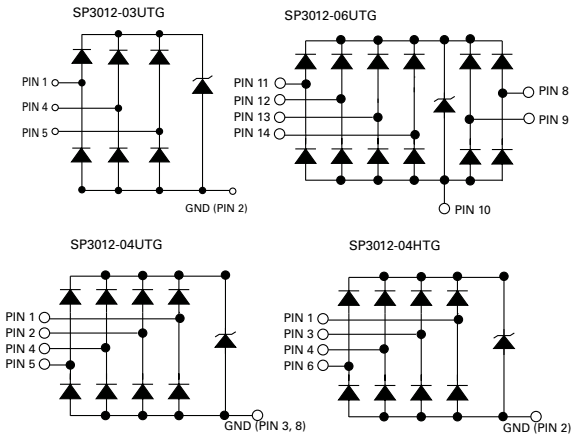
SP3012-06UTG (AEC-Q101 Qualified)

*Pins 1, 2, 3, 4, 5, 6, 7 are not internally connected but should be connected to the opposite pin with the PCB trace.



SP3012-04HTG

Functional Block Diagram



Additional Information

Datasheet | **Resources** | **Samples**

Description

The SP3012 Series integrates either 3, 4 or 6 channels of ultra low capacitance rail-to-rail diodes and an additional zener diode to provide protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust devices can safely absorb repetitive ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (±8kV contact discharge) without performance degradation.

The extremely low loading capacitance also makes it ideal for protecting high speed signal lines such as USB3.0, HDMI, USB2.0, and eSATA.

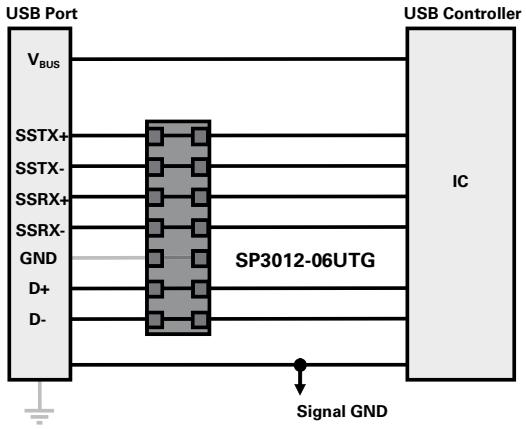
Features

- ESD, IEC 61000-4-2, ±12kV contact, ±25kV air
- EFT, IEC 61000-4-4, 40A (t_P=5/50ns)
- Lightning, IEC 61000-4-5 2nd edition, 4A (t_P=8/20µs)
- Low capacitance of 0.5pF (TYP) per I/O
- Low leakage current of 1.5µA (MAX) at 5V
- Small form factor µDFN (JEDEC MO-229) and SOT23-6 (JEDEC MO-178AB) packages provide flow through routing to simplify PCB layout
- AEC-Q101 Qaulified (µDFN10 and µDFN14)
- RoHS compliant and lead-free

Applications

- LCD/PDP TVs
- External Storages
- DVD/Blu-ray Players
- Desktops
- MP3/PMP
- Set Top Boxes
- Smartphones
- Ultrabooks/Notebooks
- Digital Cameras
- Automotive Electronics

Application Example for USB3.0



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Revised: 12/08/16

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	4.0	A
T_{OP}	Operating Temperature	-40 to 125	°C
T_{STOR}	Storage Temperature	-55 to 150	°C

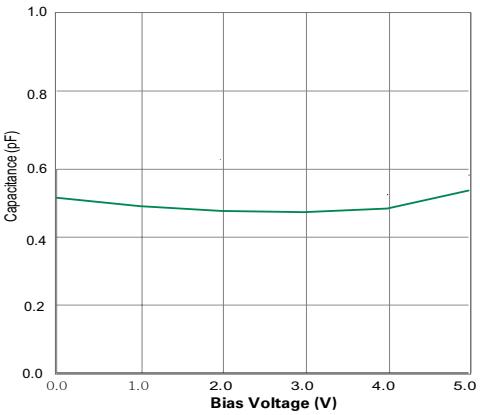
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics (T_{OP}=25°C)

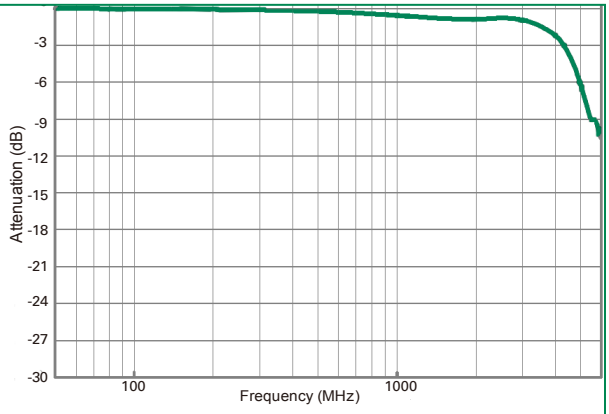
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			5.0	V
Reverse Leakage Current	I_{LEAK}	V_R=5V, Any I/O to GND			1.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		6.6	7.9	V
		I_{PP}=2A, t_p=8/20µs, Fwd		7.0	8.4	V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		0.4		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±12			kV
		IEC61000-4-2 (Air)	±25			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V, f=1 MHz		0.5	0.65	pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V, f=1 MHz		0.3	0.4	pF

Note: [1] Parameter is guaranteed by design and/or device characterization.

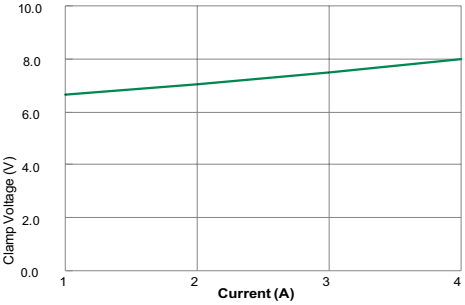
Capacitance vs. Bias Voltage



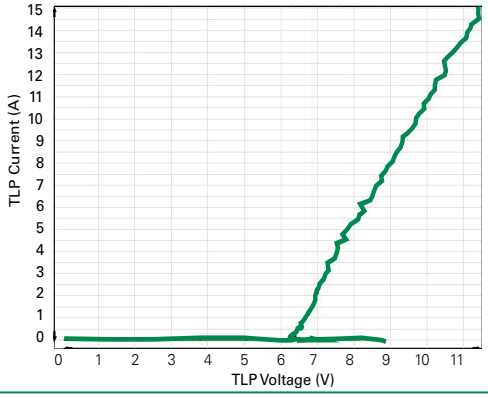
Insertion Loss (S21) I/O to GND



Clamping Voltage vs. I_{PP}



Transmission Line Pulsing(TLP) Plot



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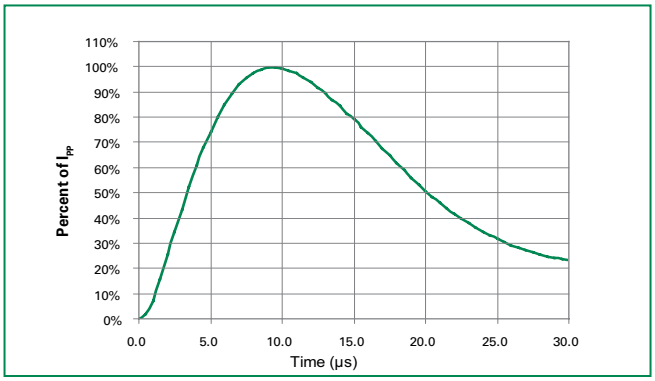
Pulse Waveform



Product Characteristics

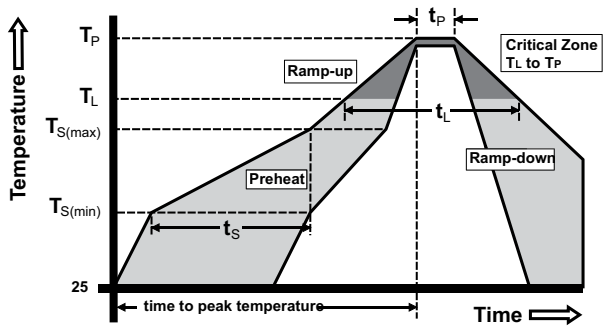
Lead Plating	Pre-Plated Frame (µDFN) Matte Tin (SOT23)
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Substitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL 94 V-0

Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3012-03UTG	µDFN-6	V*3	3000
SP3012-04UTG	µDFN-10	V*4	3000
SP3012-06UTG	µDFN-14	V*6	3000
SP3012-04HTG	SOT23-6	V*4	3000

Part Numbering System

SP 3012 - xx x T G

- SP 3012 — TVS Diode Arrays (SPA® Diodes); Series
- xx — Number of Channels: 03 = 3 channel, 04 = 4 channel, 06 = 6 channel
- x — Package: U= µDFN-6 (1.6x1.6mm), µDFN-10 (2.5x1.0mm), µDFN-14 (3.5x1.35mm); H= SOT23-6 (3.0x1.75mm)
- T — T= Tape & Reel
- G — G= Green

Part Marking System

V * *

- V — Product Series: V = SP3012
- * — Assembly Site
- * — Number of Channels: 3 = 3 channel, 4 = 4 channel, 6 = 6 channel

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Application Information

Signal Integrity of High-Speed Data Interfaces

Adding external ESD protection to a high-speed data port is not trivial for a variety of reasons.

1. ESD protection devices will add parasitic capacitance to each data line from line to GND and line to line causing impedance mismatches between the differential pairs. This ultimately affects the signal eye-diagram and whether or not the transceiver can distinguish a "1" from a "0".

2. ESD devices should be placed as close as possible to the port being protected to maximize their effect (i.e. clamping capability) and minimize the effect that PCB trace inductance can have during an ESD transient. Depending on the package size and pinout this could be challenging and the bigger the package, the larger the land pattern must be, which adds more parasitic capacitance.

3. Stub traces can add another element of discontinuity adversely affecting signal integrity so ESD protection is best employed when it's "overlaid" on the data lines or when the signals can simply pass underneath the device.

Taking all of this into account Littelfuse developed the SP3012 Series which was designed specifically for protection of high-speed data ports such as HDMI 1.3/1.4 and USB 3.0. They present less than 0.5pF from line to GND and only 0.3pF from line to line minimizing impedance mismatch between the differential pairs.

Furthermore, the SP3012 is rated up to ±12kV (contact discharge) which far exceeds the maximum requirement of the IEC 61000-4-2 standard.

There are two options available (4 channel and 6 channel) and both are housed in leadless µDFN packages so the data lines can pass directly underneath the device to reduce discontinuities and maintain signal integrity.

USB 3.0 Eye Diagram Data

Figure 1 shows the layout used for the SP3012-06UTG in a USB 3.0 application. The traces routed toward the top are the two legacy USB 2.0 lines (D+/D-) that run at the slower speed of 480Mbps and therefore are not as critical as the 5Gbps Super-Speed traces.

Figure 1: PCB Layout of the SP3012-06UTG for USB 3.0

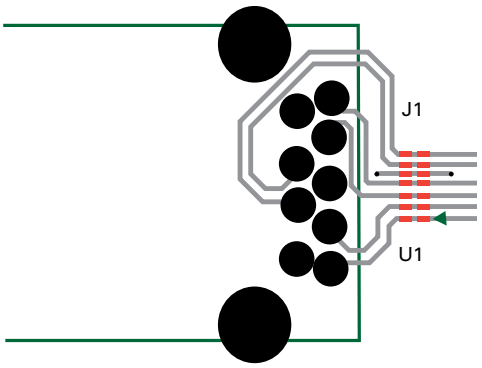


Figure 2 shows the USB 3.0 eye diagram that resulted from the PCB layout above with the SP3012-06UTG soldered on the landing pattern.

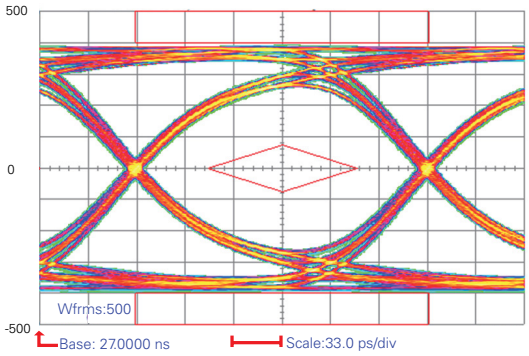


Figure 2: USB 3.0 Eye Diagram with the SP3012-06UTG

Using a similar layout as above, Figure 3 shows the eye diagram that resulted using the SP3012-04UTG to protect the Super-Speed data lines and the SP3003-02UTG to protect the legacy data pair.

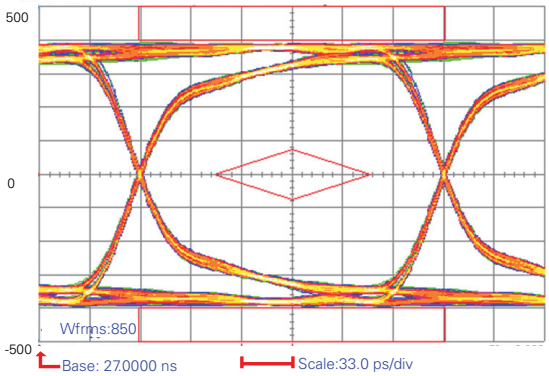
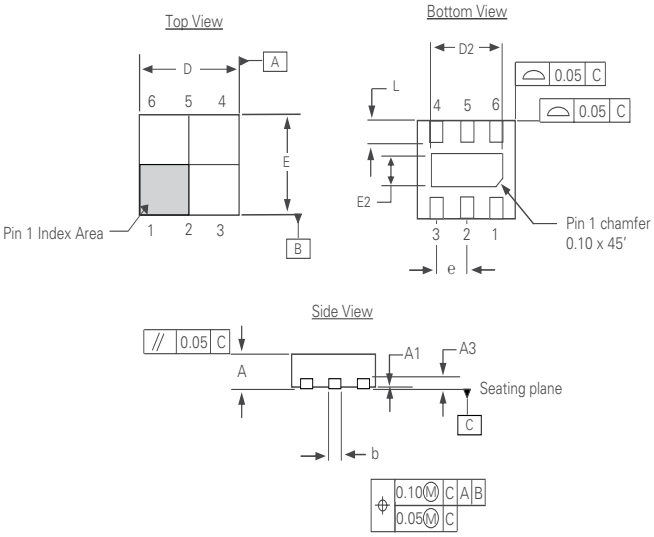


Figure 3: USB 3.0 Eye Diagram with the SP3012-04UTG

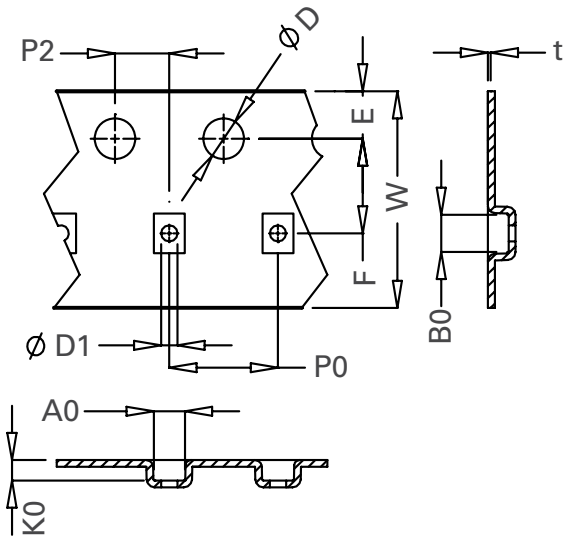
Revised: 12/08/16

Package Dimensions — µDFN-6



Package	µDFN-6 (1.6x1.6x0.5mm)			
JEDEC	MO-229			
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
A3	0.152Ref		0.006 Ref	
b	0.20	0.30	0.008	0.012
D	1.55	1.65	0.061	0.065
D2	1.05	1.30	0.042	0.052
E	1.50	1.70	0.060	0.067
E2	0.40	0.65	0.016	0.026
e	0.50 BSC		0.020BSC	
L	0.164	0.316	0.006	0.012

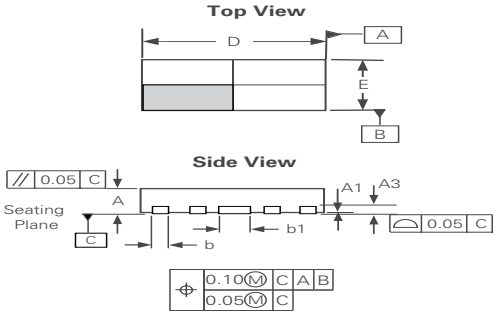
Embossed Carrier Tape & Reel Specification — µDFN-6



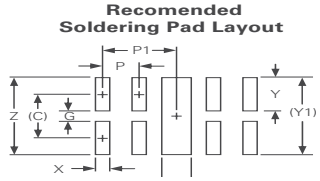
Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.06	0.07
F	3.45	3.55	0.14	0.14
D1	1.00	1.25	0.04	0.05
D	1.50 MIN		0.06 MIN	
P0	3.90	4.10	0.15	0.16
10P0	40.0+/- 0.20		1.57+/-0.01	
W	7.90	8.30	0.31	0.33
P2	1.95	2.05	0.08	0.08
A0	1.78	1.88	0.07	0.07
B0	1.78	1.88	0.07	0.07
K0	0.84	0.94	0.03	0.04
t	0.25 TYP		0.01 TYP	

Revised: 12/08/16

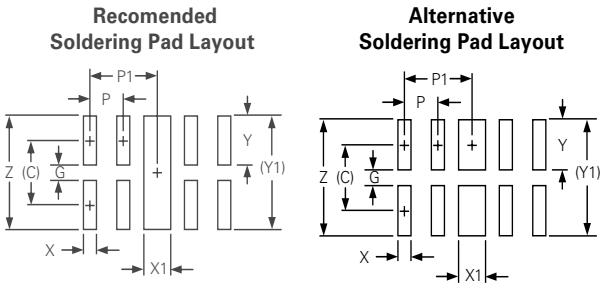
Package Dimensions — µDFN-10 (2.5x1.0x0.5mm)



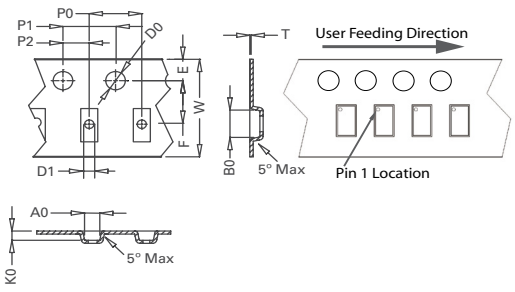
Package	µDFN-10 (2.5x1.0x0.5mm)					
JEDEC	MO-229					
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.48	0.515	0.55	0.019	0.020	0.021
A1	0.00	--	0.05	0.000		0.022
A3	0.125 Ref			0.005 Ref		
b	0.15	0.20	0.25	0.006	0.008	0.012
b1	0.35	0.40	0.45	0.014	0.016	0.018
D	2.40	2.50	2.60	0.094	0.098	0.102
E	0.90	1.00	1.10	0.035	0.039	0.043
e	0.50 BSC			0.020 BSC		
L	0.30	0.365	0.43	0.012	0.014	0.016



Soldering Pad Layout Dimensions		
	Inch	Millimeter
C	(0.034)	(0.875)
G	0.008	0.20
P	0.020	0.50
P1	0.039	1.00
X	0.008	0.20
X1	0.016	0.40
Y	0.027	0.675
Y1	(0.061)	(1.55)
Z	0.061	1.55



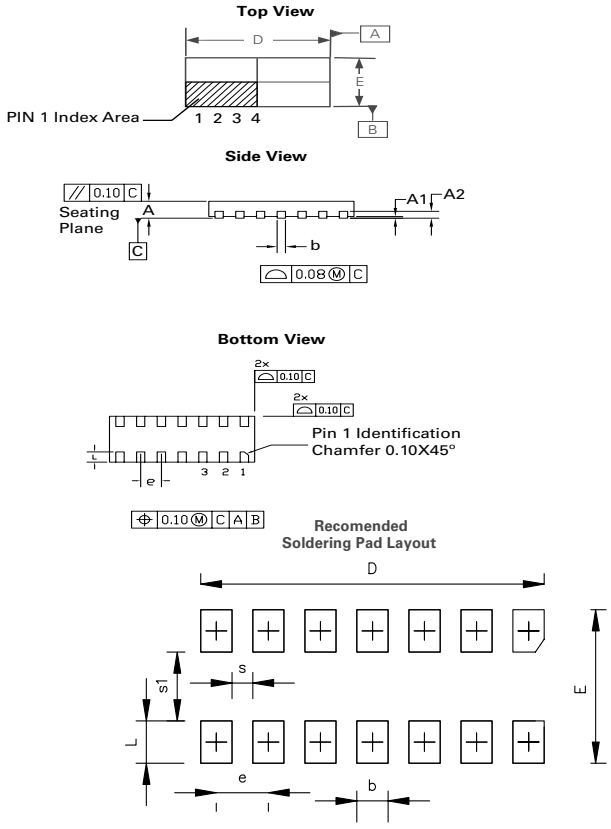
Embossed Carrier Tape & Reel Specification — µDFN-10



Package	µDFN-10 (2.5x1.0x0.5mm)
Symbol	Millimeters
A0	1.30 +/- 0.10
B0	2.83 +/- 0.10
D0	Ø 1.50 + 0.10
D1	Ø 1.00 + 0.25
E	1.75 +/- 0.10
F	3.50 +/- 0.05
K0	0.65 +/- 0.10
P0	4.00 +/- 0.10
P1	4.00 +/- 0.10
P2	2.00 +/- 0.05
T	0.254 +/- 0.02
W	8.00 + 0.30 /- 0.10

Revised: 12/08/16

Package Dimensions — µDFN-14 (3.5x1.35x0.5mm)



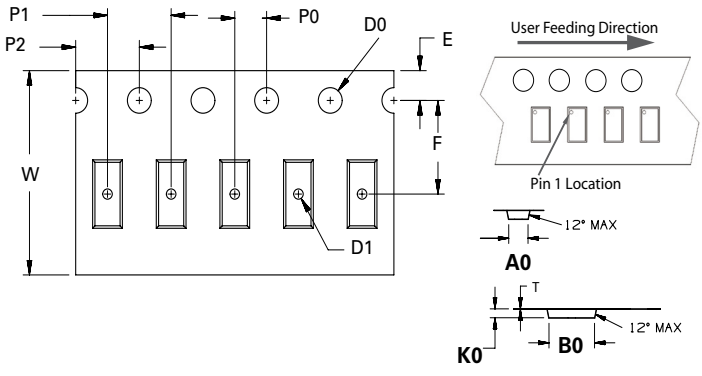
µDFN-14 (3.5x1.35x0.5mm) JEDEC MO-229						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2		0.203 Ref			0.008 Ref	
b	0.15	0.20	0.25	0.006	0.008	0.012
D	3.40	3.50	3.60	0.134	0.138	0.142
D2	-	-	-	-	-	-
E	1.25	1.35	1.45	0.050	0.054	0.058
E1	-	-	-	-	-	-
e		0.500 BSC			0.020 BSC	
L	0.25	0.30	0.35	0.010	0.012	0.014

Notes:

1. Dimension and tolerancing comform to ASME Y14.5M-1994.
2. Controlling dimensions: Millimeter. Converted Inch dimensions are not necessarily exact.

Soldering Pad Layout Dimensions		
Symbol	Millimeters	Inches
	Nom	Nom
D	3.30	0.1299
E	1.65	0.0571
b	0.30	0.0118
L	0.50	0.0197
e	0.50 typ	0.020 typ
s	0.20	0.0078
s1	0.65	0.0256

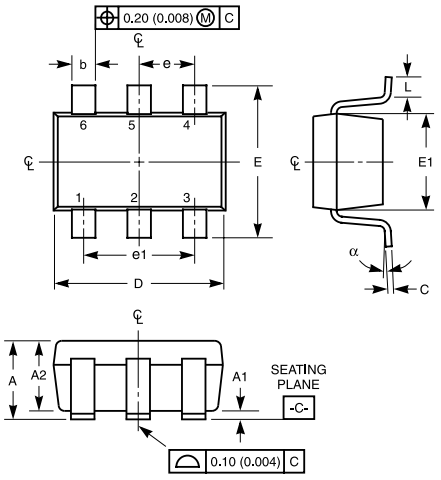
Embossed Carrier Tape & Reel Specification — µDFN-14



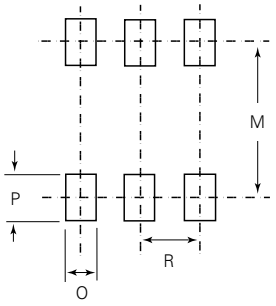
Symbol	Millimeters
A0	1.58 +/- 0.10
B0	3.73 +/- 0.10
D0	Ø 1.50 + 0.10
D1	Ø 0.60 +/- 0.05
E	1.75 +/- 0.10
F	5.50 +/- 0.05
K0	0.68 + 0.12/ -0.10
P0	2.00 +/- 0.05
P1	4.00 +/- 0.10
P2	4.00 +/- 0.10
T	0.28 +0.02/ -0.05
W	12.00 + 0.30 /- 0.10

Revised: 12/08/16

Package Dimensions — SOT23-6



Recommended Solder Pad Layout

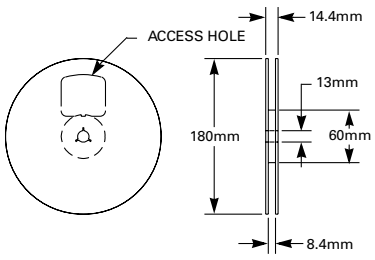


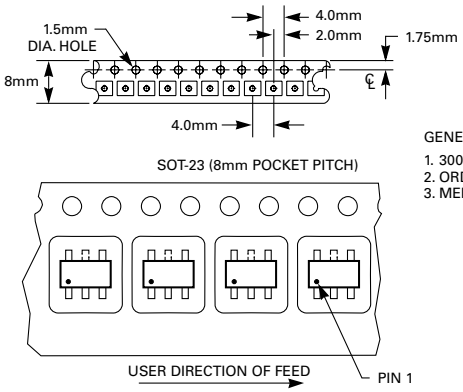
Package	SOT23				
Pins	6				
JEDEC	MO-178AB				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	0.900	1.450	0.035	0.057	-
A1	0.000	0.150	0.000	0.006	-
A2	0.900	1.300	0.035	0.051	-
b	0.350	0.500	0.0138	0.0196	-
C	0.080	0.220	0.0031	0.009	-
D	2.800	3.000	0.11	0.118	3
E	2.600	3.000	0.102	0.118	-
E1	1.500	1.750	0.06	0.069	3
e	0.95 Ref		0.0374 ref		-
e1	1.9 Ref		0.0748 Ref		-
L	0.30	0.600	0.012	0.023	4,5
N	6		6		6
a	0°	8°	0°	8°	-
M		2.590		0.102	-
O		0.690		.027 TYP	-
P		0.990		.039 TYP	-
R		0.950		0.038	-

Notes:
1. Dimensioning and tolerancing Per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 (1992).
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Foot length L measured at reference to seating plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Embossed Carrier Tape & Reel Specification — SOT23-6

8mm TAPE AND REEL





GENERAL INFORMATION

1. 3000 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revised: 12/08/16